In the Claims

1-45. (Canceled)

46. (Original) A method of reading a memory cell, comprising:

applying a potential difference (V_{DIFF}) to a selected memory cell by providing a column potential (V_C) on a column line and a row potential (V_R) on a row line;

increasing V_{DIFF} by an increment less than a transistor threshold voltage (V_T); and

determining whether the increased V_{DIFF} results in a current flow on the column line for the selected memory cell.

47. (Original) The method of claim 46, wherein applying a potential difference (V_{DIFF}) to a selected memory cell includes applying V_C and V_R across a resistive load inverter in the selected memory cell.

48. (Currently Amended) The method of claim 47, wherein applying V_C and V_R across a resistive load inverter includes:

applying V_C and V_R across an NMOS resistive load inverter; and

increasing V_{DIFF} by an increment less than a transistor threshold voltage (V_T), including: ~~includes:~~

maintaining a constant $V_{C;}$ and

decreasing V_R by an increment less than an NMOS transistor threshold voltage (V_{TN}).

49. (Original) The method of claim 46, wherein increasing V_{DIFF} by an increment less than a transistor threshold voltage V_T includes decreasing V_R by an increment less than a transistor threshold voltage V_T.

50. (Original) A method of writing a memory cell, comprising:

applying a potential difference (V_{DIFF}) to a selected memory cell by providing a column potential (V_C) on a column line and a row potential (V_R) on a row line; and

increasing V_{DIFF} by an increment more than a transistor threshold voltage (V_T) to set the selected memory cell to a one state.

51. (Original) The method of claim 50, wherein applying a potential difference (V_{DIFF}) to a selected memory cell includes applying V_C and V_R across a resistive load inverter in the selected memory cell.

52. (Currently Amended) The method of claim 51, wherein applying V_C and V_R across a resistive load inverter includes:

applying V_C and V_R across an NMOS resistive load inverter; and

increasing V_{DIFF} by an increment more than a transistor threshold voltage (V_T), including: ~~includes:~~

maintaining a constant V_C; and

decreasing V_R by an increment more than an NMOS transistor threshold voltage (V_{TN}).

53. (Original) The method of claim 50, wherein increasing V_{DIFF} by an increment more than a transistor threshold voltage V_T includes decreasing V_R by an increment more than a transistor threshold voltage V_T.

54. (Original) The method of claim 50, wherein decreasing V_{DIFF} by an increment more than V_T resets the selected memory cell to a zero state.

55. (Original) The method of claim 54, wherein decreasing V_{DIFF} by an increment more than V_T to reset the selected memory cell includes increasing V_R by an increment more than V_T.

56. (Original) A method of operating a memory array, comprising:

applying a potential difference (V_{DIFF}) to each of a plurality of memory cells by providing a column potential (V_C) on a column line and a row potential (V_R) on a row line;

resetting a first selected memory cell to a zero state by decreasing V_{DIFF} by an increment more than a transistor threshold voltage (V_T) to reset the selected memory cell to a zero state;

writing a second selected memory cell to a one state by increasing V_{DIFF} by an increment more than V_T to set the selected memory cell to the one state; and

reading a third selected memory cell by:

increasing V_{DIFF} by an increment less than V_T; and

determining whether the increased V_{DIFF} results in a current flow on the column line for the selected memory cell.

57. (Original) The method of claim 56, wherein applying a potential difference (V_{DIFF}) in each of a plurality of memory cells includes applying V_C and V_R across a resistive load inverter in each of the plurality of memory cells.

58. (Original) The method of claim 57, wherein:

applying V_C and V_R across a resistive load inverter includes applying V_C and V_R across an NMOS resistive load inverter; and

writing a second selected memory cell by increasing V_{DIFF} by an increment more than a transistor threshold voltage (V_T) includes:

maintaining a constant V_C; and

decreasing V_R by an increment more than an NMOS transistor threshold voltage (V_{TN}).

59. (Original) The method of claim 56, wherein writing a second selected memory cell by increasing V_{DIFF} by an increment more than a transistor threshold voltage V_T includes decreasing V_R by an increment more than a transistor threshold voltage V_T.

60. (Original) The method of claim 56, wherein resetting a first selected memory cell includes resetting a row of cells by adjusting V_R by an increment larger than V_T.

61. (Original) The method of claim 56, wherein writing a second selected memory cell to a one state by increasing V_{DIFF} by an increment more than V_T includes:

adjusting V_R for a write operation by an increment greater than a transistor threshold voltage to turn a first transistor on for cells within a selected row; and

adjusting a second column potential V_C on a second column line by an amount to prevent a second transistor in the selected row from turning on in response to adjusting the row potential for the write operation.

62. (Original) The method of claim 56, wherein reading a third selected memory cell includes:

decreasing V_R by an increment less than a transistor threshold voltage increment; and

determining if the decreased V_R results in a current flow on a corresponding column line for the memory cell.

63-71. (Canceled)

72. (Previously Presented) A method of forming a SRAM circuit, comprising:

providing a memory array, a controller, a row line voltage generator, a column line voltage generator, and a column line current detector;

coupling the controller to the row line voltage generator, the column line voltage generator, and the column line current detector;

coupling the row line voltage generator to row lines within the memory array such that the controller is able to vary a potential on a selected row line;

coupling the column line voltage generator to column lines within the memory array such that the controller is able to vary a potential on one or more selected column lines; and

coupling the column line current detector to the column lines within the memory array such that the controller is able to determine current flow on a selected column line.

73. (Previously Presented) The method of claim 72, wherein providing a memory array includes providing a plurality of memory cells, each cell being provided by:

forming a PMOS transistor with a gate;

forming an NMOS transistor with a gate;

coupling the PMOS transistor gate in series with the NMOS transistor; and

coupling the NMOS transistor gate in series with the PMOS transistor.

74. (Currently Amended) The method of claim 73, wherein ~~forming a memory cell by~~ forming a PMOS transistor with a gate and forming an NMOS transistor with a gate includes forming a lightly doped polysilicon gate for both the PMOS transistor and the NMOS transistor.

75. (Previously Presented) The method of claim 73, further including:

coupling the PMOS transistor and the NMOS transistor gate between a PWRP power supply and a first reference line; and

coupling the NMOS transistor and the PMOS transistor gate between a PWRN power supply and a second reference line.

76. (Previously Presented) The method of claim 73, further including:

coupling the PMOS transistor and the NMOS transistor gate between a constant power supply and a ground reference line; and

coupling the NMOS transistor and the PMOS transistor gate between a column line with an adjustable potential and a row line with an adjustable potential.

Conclusion

Claims 48, 52, and 74 have been amended for clarity. It is respectfully submitted that these changes do not introduce new matter, and the claims are allowable without further search or consideration. Therefore, entry is appropriate under Rule 312, and is respectfully requested.

Respectfully submitted,

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